**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1 (cancel).

2 (currently amended). ~~[The process of claim 1,]~~ A semiconductor fabrication process, comprising:

forming a gate electrode over a gate dielectric over a semiconductor substrate;

thermally depositing, at a temperature in the range of approximately 550 to 750 °C, a silicon nitride spacer film over the gate electrode, the deposited spacer film exhibiting a first tensile stress;

modulating a stress characteristic of at least a portion of the spacer film from the first tensile stress to a second tensile stress; and

etching the spacer film to form sidewall spacers laterally disposed on either side of the gate electrode, wherein at least a portion of the sidewall spacers include sidewall spacers exhibiting the second tensile stress.

~~[wherein depositing the spacer film comprises thermally depositing silicon nitride at a temperature in the range of approximately 550 to 750 °C.]~~

3 (currently amended). The process of claim [1] 2, wherein modulating the stress characteristic comprises implanting a species into at least a portion of the spacer film.

4 (currently amended). ~~[The process of claim 3,]~~ A semiconductor fabrication process, comprising:

forming a gate electrode over a gate dielectric over a semiconductor substrate;

depositing a spacer film over the gate electrode, the deposited spacer film exhibiting a first tensile stress;

modulating a stress characteristic of at least a portion of the spacer film from the first tensile stress to a second tensile stress; and

etching the spacer film to form sidewall spacers laterally disposed on either side of the gate electrode, wherein at least a portion of the sidewall spacers include sidewall spacers exhibiting the second tensile stress;

wherein modulating the stress characteristic comprises implanting Xenon into at least a portion of the spacer film.

~~[wherein the ion implanting includes implanting Xenon into at least a portion of the spacer film]~~.

5 (original). The process of claim 4, wherein implanting Xenon further includes implanting Xenon into portions of the spacer film over p-channel transistors.

6 (original). The process of claim 5, wherein implanting Xenon still further includes implanting Xenon at an energy of at least 180 keV.

7 (original). The process of claim 5, wherein implanting Xenon still further includes implanting at an implant angle of approximately 45°.

8 (original). The process of claim 3, wherein the ion implanting includes implanting Germanium into the spacer film.

9 (original). The process of claim 8, wherein implanting Germanium further includes implanting Germanium at an energy of at least 80 keV and an implant angle of approximately 10°.

10-11 (cancel).

12 (currently amended). The process of claim ~~[11]~~ 13, wherein depositing silicon nitride still further includes depositing silicon nitride with a thermal CVD process in which the deposition temperature is in the range of approximately 550 to 750 °C.

13 (currently amended). ~~[The process of claim 11,]~~ A semiconductor fabrication process, comprising:

depositing a silicon nitride spacer film exhibiting a first tensile stress characteristic over a gate electrode and a semiconductor substrate over which the gate electrode is positioned;

etching the spacer film to form silicon nitride spacers on sidewalls of the gate electrode; and

implanting at least some of the sidewall spacers with an implant species ~~[wherein implanting at least some of the sidewall spacers still further includes implanting a species]~~ selected from Xenon and Germanium ~~[into the at least some of the sidewall~~

~~spacers]~~ using an implant angle of 10° or greater to modulate a stress characteristic of the implanted spacers.

14 (original). The process of claim 13, wherein implanting at least some of the sidewall spacers still further includes implanting with an implant energy not less than 80 keV.

15 (currently amended). ~~[The process of claim 11,]~~ A semiconductor fabrication process, comprising:

depositing a silicon nitride spacer film exhibiting a first tensile stress characteristic over a gate electrode and a semiconductor substrate over which the gate electrode is positioned;

etching the spacer film to form silicon nitride spacers on sidewalls of the gate electrode; and

selectively implanting at least some of the sidewall spacers of n-channel transistors with an Xenon ions at an implant energy of approximately 180 keV and an implant angle of approximately 45 °C to modulate a stress characteristic of the implanted spacers

~~[wherein implanting at least some of the sidewall spacers still further includes selectively implanting portions of at least some of the sidewall spacers of n-channel transistors with Xenon ions at an implant energy of approximately 180 keV and an implant angle of approximately 45°]~~.

16 (currently amended). [The process of claim 10,] A semiconductor fabrication process, comprising:

depositing a silicon nitride spacer film over a gate electrode and a semiconductor substrate over which the gate electrode is positioned;

etching the spacer film to form silicon nitride spacers on sidewalls of the gate electrode; and

blanket implanting at least some of the sidewall spacers with Germanium at an implant energy of 80 keV and an implant angle of approximately 10° to modulate a stress characteristic of the implanted spacers

~~[wherein implanting the at least some of the sidewall spacers still further includes blanket implanting the at least some of the sidewall spacers with Germanium at an implant energy of 80 keV and an implant angle of approximately 10°]~~.

17-20 (cancel).